FAIRCHILD SEMICONDUCTOR®

September 2007

FDMJ1032C

Dual N & P-Channel PowerTrench® MOSFET

N-Channel: 20V, 3.2A, 90mΩ P-Channel: -20V, -2.5A, 160mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 90mΩ at V_{GS} = 4.5V, I_D = 3.2A
- Max $r_{DS(on)}$ = 130mΩ at V_{GS} = 2.5V, I_D = 2.5A

Q2: P-Channel

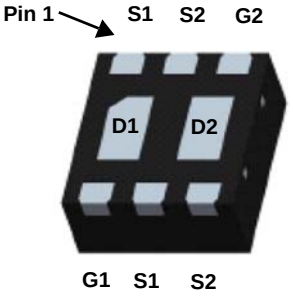
- Max $r_{DS(on)}$ = 160mΩ at V_{GS} = -4.5V, I_D = -2.5A
- Max $r_{DS(on)}$ = 230mΩ at V_{GS} = -2.5V, I_D = -2.0A
- Max $r_{DS(on)}$ = 390mΩ at V_{GS} = -1.8V, I_D = -1.0A
- Low gate charge, high power and current handling capability
- RoHS Compliant

General Description

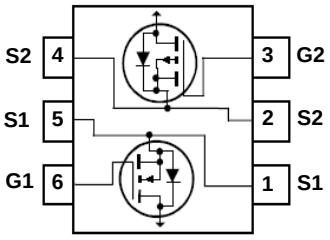
This dual N and P-Channel enhancement mode Power MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

Application

- Battery management



SC-75 MicroFET



MOSFET Maximum Ratings T_A= 25°C unless otherwise noted

Symbol	Parameter			Q1	Q2	Units
V_{DS}	Drain to Source Voltage			20	-20	V
V_{GS}	Gate to Source Voltage			±12	±8	V
I_D	Drain Current - Continuous	T_A = 25°C		3.2	-2.5	A
	- Pulsed			12	-12	
P_D	Power Dissipation for Single Operation	T_A = 25°C	(Note 1a)	1.4		W
		T_A = 25°C	(Note 1b)	0.8		
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Single Operation	(Note 1a)	89	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Single Operation	(Note 1b)	182	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
032	FDMJ1032C	SC-75 MicroFET	7"	8mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

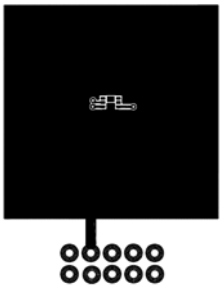
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V I_D = -250μA, V_{GS} = 0V	Q1 Q2	20 -20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C I_D = -250μA, referenced to 25°C	Q1 Q2		13 -13		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16V, V_{GS} = 0V V_{DS} = -16V, V_{GS} = 0V	Q1 Q2			1 -1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±12V, V_{DS} = 0V V_{GS} = ±8V, V_{DS} = 0V	Q1 Q2			±100	nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA V_{GS} = V_{DS}, I_D = -250μA	Q1 Q2	0.6 -0.4	1.1 -0.8	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C I_D = -250μA, referenced to 25°C	Q1 Q2		-3 3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 4.5V, I_D = 3.2A V_{GS} = 2.5V, I_D = 2.5A V_{GS} = 4.5V, I_D = 3.2A, T_J = 125°C	Q1		70 100 83	90 130 132	mΩ
		V_{GS} = -4.5V, I_D = -2.5A V_{GS} = -2.5V, I_D = -2.0A V_{GS} = -1.8V, I_D = -1.0A V_{GS} = -4.5V, I_D = -2.5A, T_J = 125°C	Q2		114 169 289 156	160 230 390 238	mΩ
g_{FS}	Forward Transconductance	V_{DD} = 5V, I_D = 3.2A V_{DD} = -5V, I_D = -2.5A	Q1 Q2		7.5 5		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1 V_{DS} = 10V, V_{GS} = 0V, f = 1MHZ Q2 V_{DS} = -10V, V_{GS} = 0V, f = 1MHZ	Q1 Q2		200 290	270 390	pF
C_{oss}	Output Capacitance		Q1 Q2		50 55	70 75	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		30 29	45 45	pF
R_g	Gate Resistance	f = 1MHz	Q1 Q2		1 5		Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GEN} = 6Ω Q2 V_{DD} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GEN} = 6Ω	Q1 Q2		7 8	14 16	ns
t_r	Rise Time		Q1 Q2		8 13	16 23	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		11 13	20 23	ns
t_f	Fall Time		Q1 Q2		2 18	4 32	ns
$Q_{g(TOT)}$	Total Gate Charge	Q1 V_{GS} = 4.5V, V_{DD} = 10V, I_D = 3.2A Q2 V_{GS} = -4.5V, V_{DD} = -10V, I_D = -2.5A	Q1 Q2		2 3	3 4	nC
Q_{gs}	Gate to Source Charge		Q1 Q2		0.4 0.6		nC
Q_{gd}	Gate to Drain “Miller” Charge		Q1 Q2		1.0 0.8		nC

Electrical Characteristics T_J = 25°C unless otherwise noted

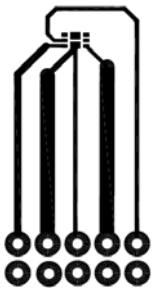
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 1.16A (Note 2) V_{GS} = 0V, I_S = -1.2A (Note 2)	Q1 Q2		0.8 -0.8	1.2 -1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 3.2A, di/dt = 100A/s	Q1 Q2		12 14		ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = -2.5A, di/dt = 100A/s	Q1 Q2		2.5 4		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 89°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 182°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

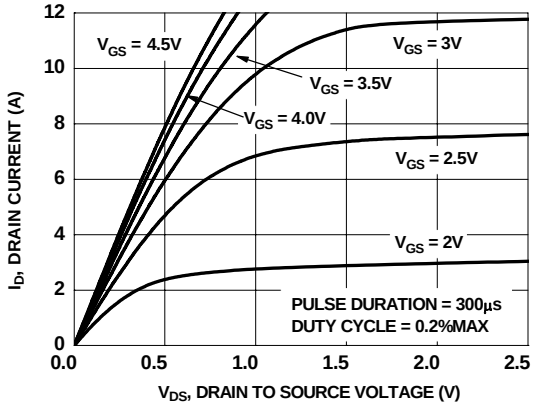


Figure 1. On- Region Characteristics

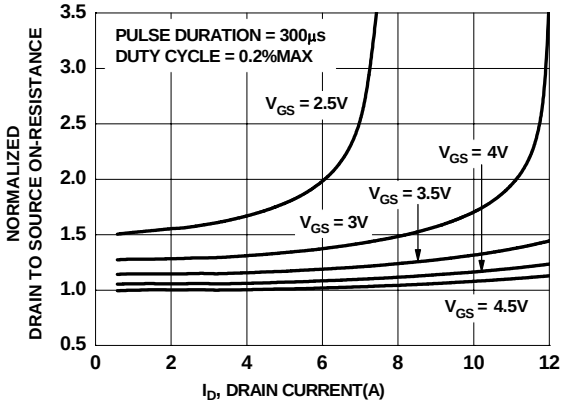


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

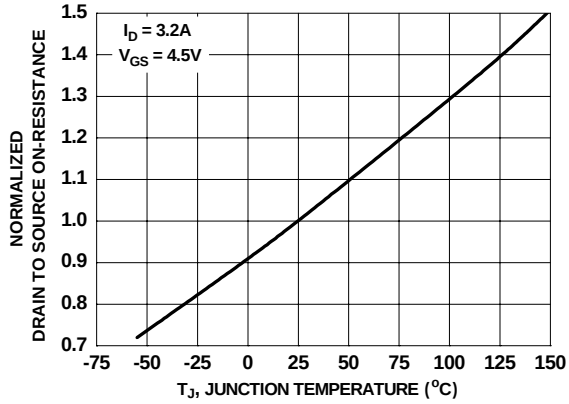


Figure 3. Normalized On-Resistance vs Junction Temperature

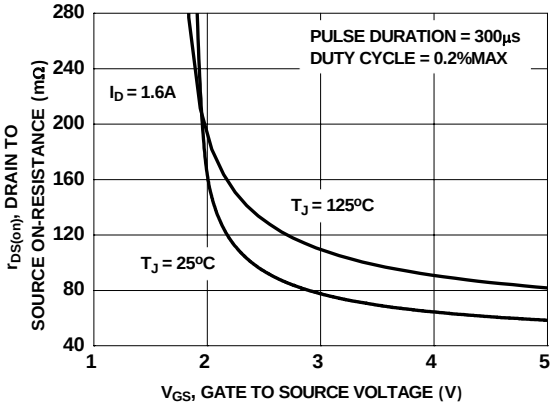


Figure 4. On-Resistance vs Gate to Source Voltage

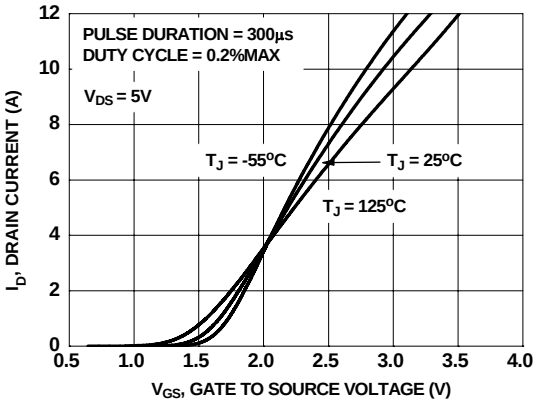


Figure 5. Transfer Characteristics

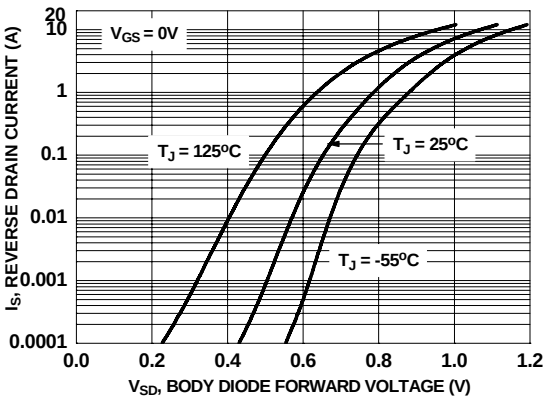


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

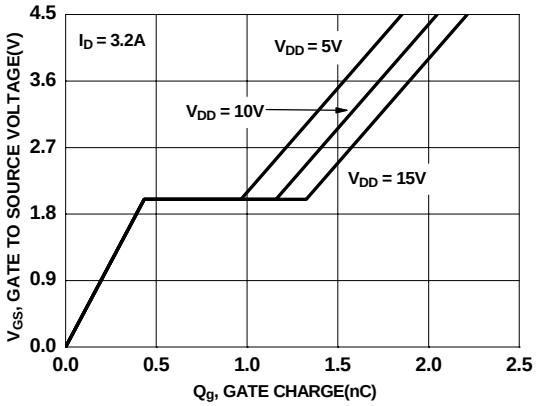


Figure 7. Gate Charge Characteristics

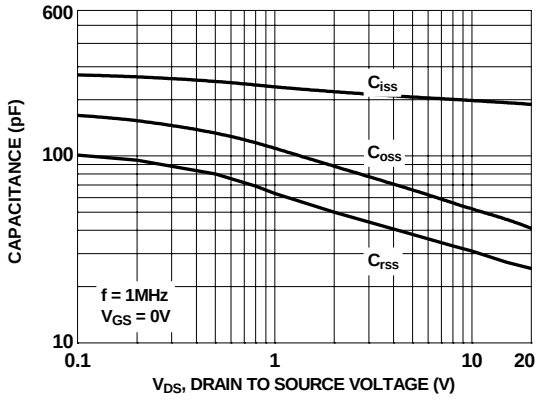


Figure 8. Capacitance vs Drain to Source Voltage

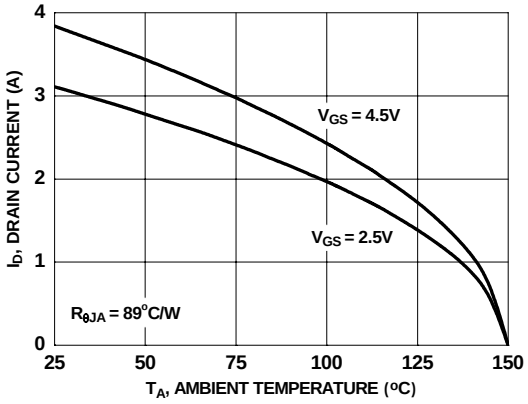


Figure 9. Maximum Continuous Drain Current vs Ambient Temperature

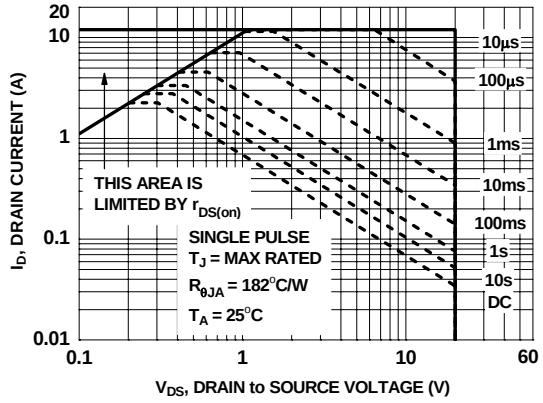


Figure 10. Forward Bias Safe Operating Area

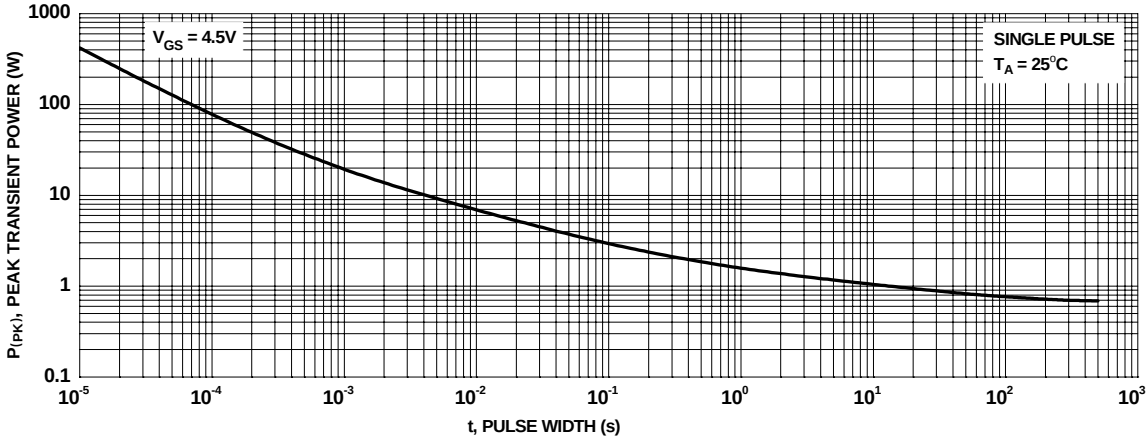


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

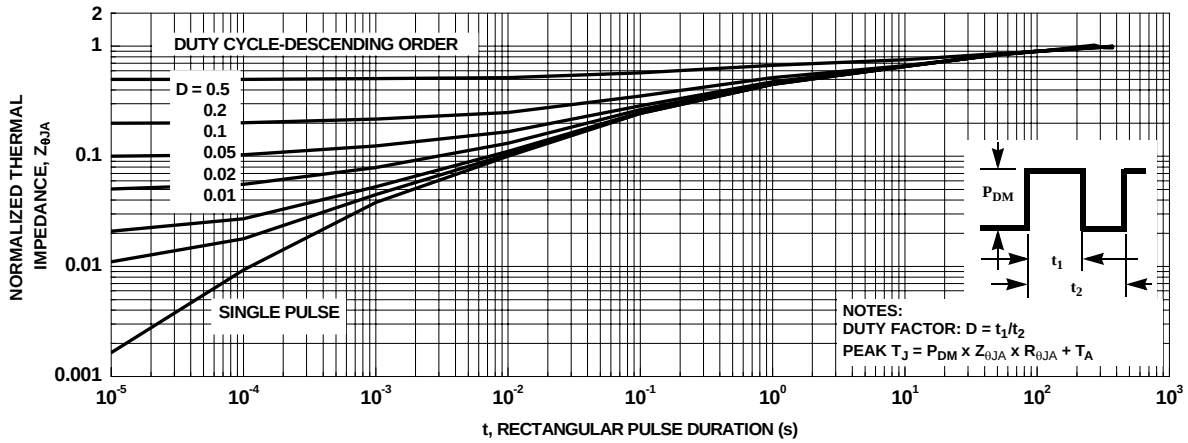


Figure 12. Transient Thermal Response Curve

Typical Characteristics (Q2 P-Channel) T_J = 25°C unless otherwise noted

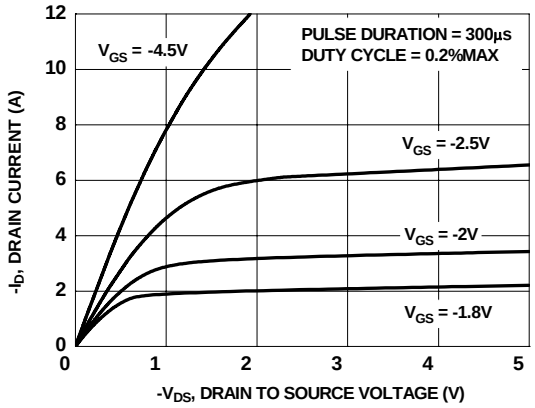


Figure 13. On- Region Characteristics

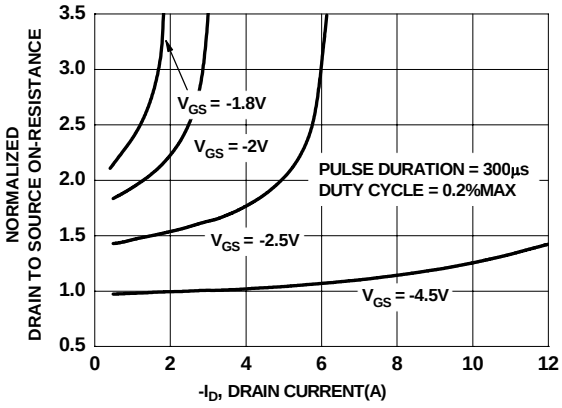


Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage

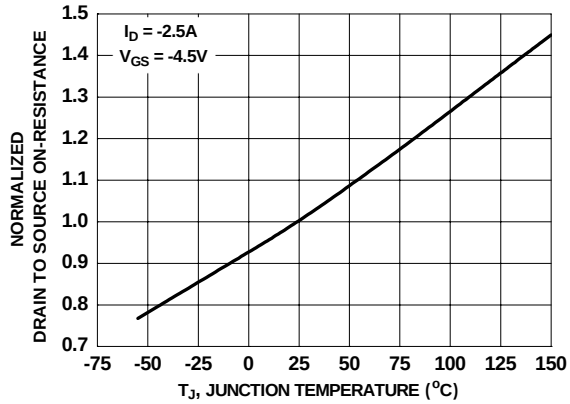


Figure 15. Normalized On-Resistance vs Junction Temperature

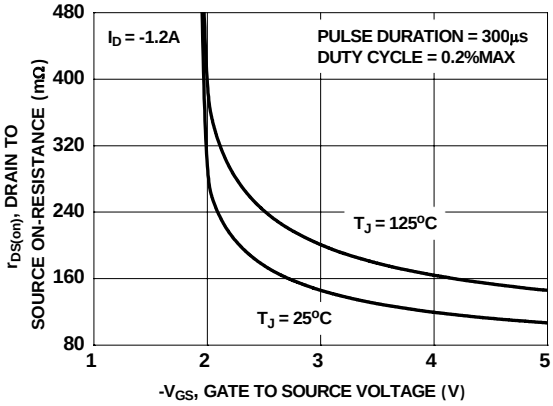


Figure 16. On-Resistance vs Gate to Source Voltage

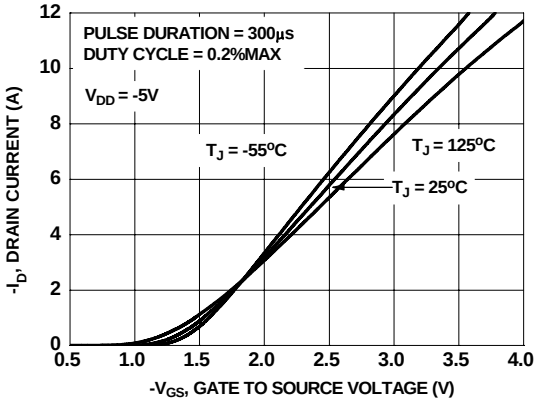


Figure 17. Transfer Characteristics

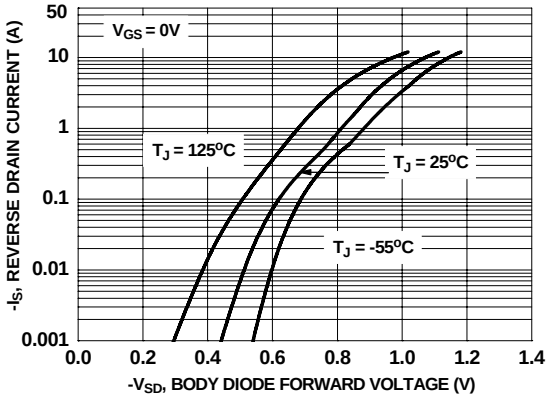


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel) T_J = 25°C unless otherwise noted

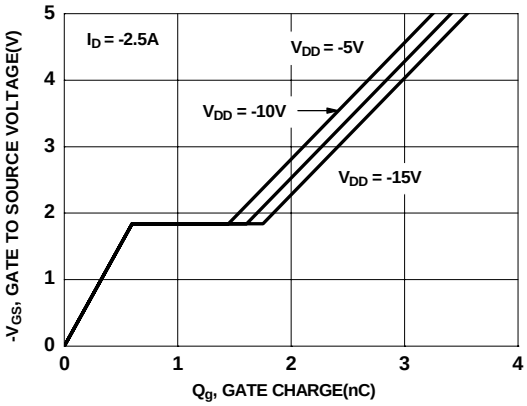


Figure 19. Gate Charge Characteristics

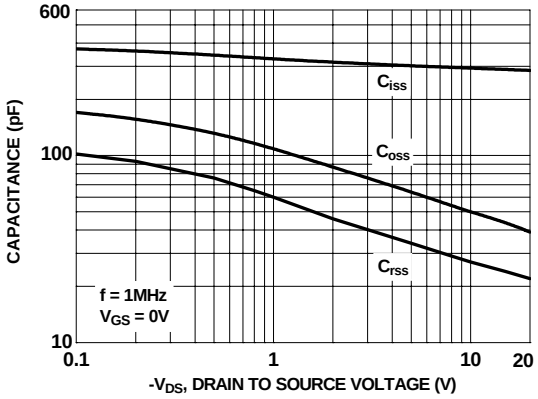


Figure 20. Capacitance vs Drain to Source Voltage

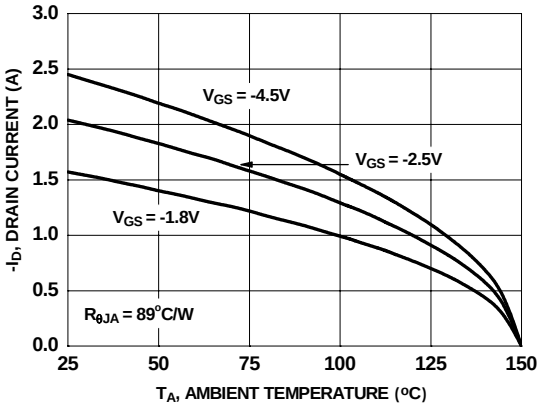


Figure 21. Maximum Continuous Drain Current vs Ambient Temperature

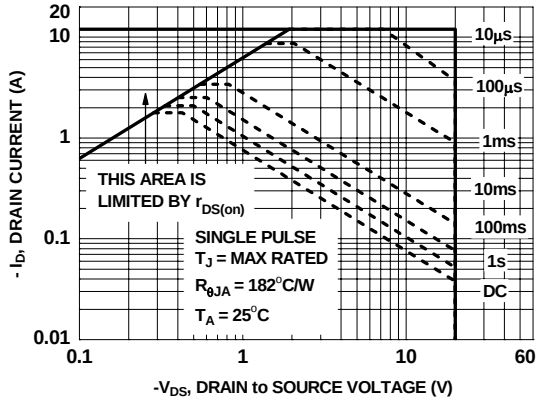


Figure 22. Forward Bias Safe Operating Area

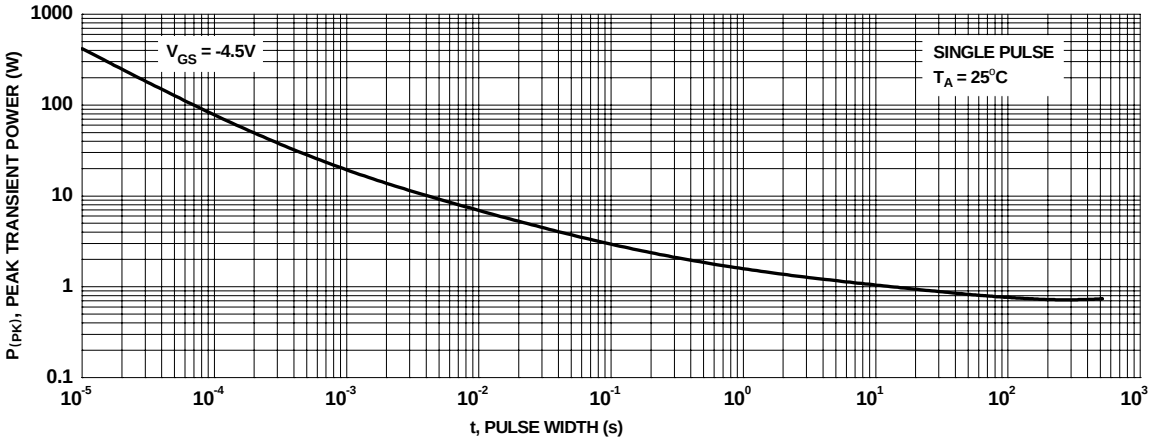


Figure 23. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel) T_J = 25°C unless otherwise noted

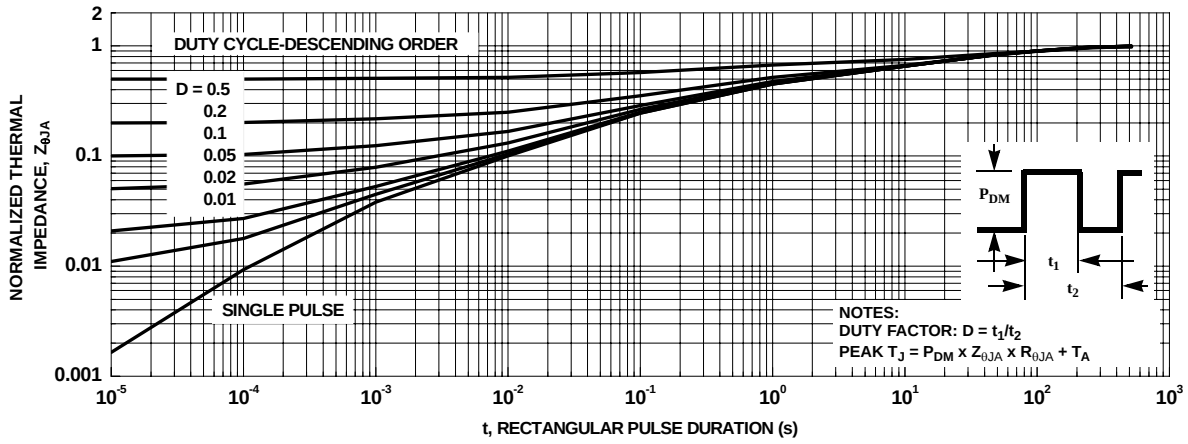
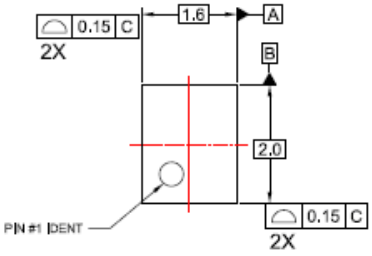
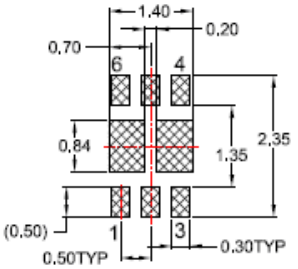


Figure 24. Transient Thermal Response Curve

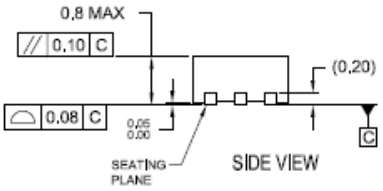
Dimensional Outline and Pad Layout



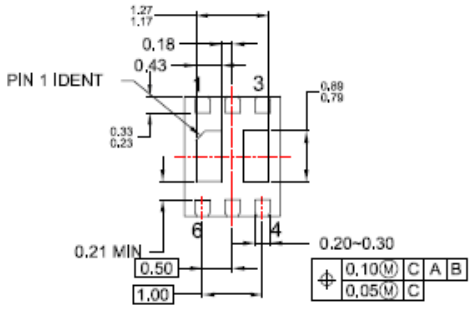
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

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Green FPS™ e-Series™
GTO™
i-Lo™
IntelliMAX™
ISOPLANAR™
MegaBuck™
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MicroFET™
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MillerDrive™
Motion-SPM™
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Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
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SuperFET™
SuperSOT™-3
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

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